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| |  |  |  |  |  | | --- | --- | --- | --- | --- | | * [WSC 2013](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz) | |  | * [My Account](https://ssl.linklings.net/conferences/wsc/?args=rJUHtGPCf40zU3b0bfPzTrAprcnt3DxGPCf40zU3b0bfPzTHQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGQttprcnt3DUHI0IQ3) * [Logout](https://ssl.linklings.net/conferences/wsc/?args=rJUHtGPCf40zU3b0bfPzTrAprcnt3DxGPCf40zU3b0bfPzTHQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTJUHtGsprcnt3Dyprcnt3DUITzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGsprcnt3DyCH0IQ3) | | |  | **WSC 2013** | | | Daniil Zorin | |  |  | | | |   Начало формы   |  |  | | --- | --- | | [My Submissions](https://ssl.linklings.net/conferences/wsc/?args=rJUHtGPCf40zU3b0bfPzTrAprcnt3DxGPCf40zU3b0bfPzTHQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGAX0zU3z0IQ3)  con310 Reviews Details |  |   **Submission:**DYANA: HLA-based Distributed Real-time Embedded Systems Simulation Tool **Contributors:**Antonenko, Chemeritskiy, Glonina, Konnov, Pashkov, Podymov, Savenkov, Smeliansky, Volkanov, Zakharov, Zorin  Key for the below column headings: show   |  |  | | --- | --- | | **Summary of reviews of con310s2** |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | | **Reviewer** | **TECSND** | **Relev.** | **ResCont** | **EngQlty** | **RelWork** | **Overall** | **Recom.** | | [Reviewer 1](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "conrev233) | Has Serious Shortcomings (2) | Relevant (4) | Minimal (1) | Major Editing Needed (2) | Poor (2) | Below Average (2) | Accept As Poster (2) | | [Reviewer 2](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "conrev510) | Cannot Judge (1) | Relevant (4) | Average (3) | Major Editing Needed (2) | Average (3) | Average (3) | Accept with Major Changes (3) | | [Reviewer 3](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "conrev529) | Has Fixable Shortcomings (3) | Relevant (4) | Minimal (1) | Minor Editing Needed (3) | Poor (2) | Below Average (2) | Accept As Poster (2) | | **Averages:** | 2.0 | 4.0 | 1.7 | 2.3 | 2.3 | 2.3 | 2.3 |   Commitee Comments [jump](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "committee_comments)   |  |  | | --- | --- | | **Review of con310s2 by Reviewer 1** | [top](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "top) |   **Summary**  This paper introduces DYANA, a HLA-based hardware-in-the-loop simulation tool. This tool is an integrated environment for development, simulation, and verification of real-time embedded systems (RTES). Particularly, this paper focuses on fully satisfying all of requirements for simulation environment of distributed real-time and embedded systems, such as modular structure of the simulation environment, distributed simulation, compatibility of modeling and verification tools, etc.  **Originality**  This paper integrates existing tools and additional new developed tools for developing, simulating, and verifying RTES. For developing RTES, authors use UML statecharts as the modeling language and ArgoUML tool as an editor. UML models are automatically translated into federates in C++ codes using new developed “UML to SCXML translator” and “Federate code generator”. Finally, generated federates are simulated in CERTI. For verifying RTES, they developed “UML to UPPAAL translator” and used an UPPAAL tool. Although their efforts on introducing integrated environment for development, simulation as well as verification are valuable and meaningful, their core parts are not innovative tools but existing things. Hence, I couldn’t find a further contribution in this paper.  **Impact**  This paper gives an interesting idea for integrated environment to develop and simulate as well as verify RTES. However, the impact of the paper might be slight because it doesn’t give any detailed information on how to utilize the proposed tool.  **Please explain in detail your evaluation of the paper.**  This paper confused me with conflicting accounts of distributed simulation and parallel simulation. As authors are mentioned, HLA is a conventional standard in the field of distributed simulation. They emphasize their contribution on improvement of CERTI for supporting multi-thread execution of models. However, the aim of multi-threading technique in a single computer is to improve the performance, such as speed-up, of parallel simulation. I don’t see what multi-threading capability of modified CERTI is related to their target system, distributed real-time and embedded system. In section 2, authors formulate key requirements for RTES simulation environment and argue that existing simulation environments do not fully satisfy all of these requirements. They should present how their proposed tool covers all of these requirements. Also, the related work needs to have more substance. In section 7, the presented case study is very brief and merely shows some results without any byproducts of each process. The case study is the most important part of the paper for underpinning capability of proposed DYANA tool. Therefore, two examples should be described more in details in order to show the relevance of the approach proposed in the paper.  In addition, some paragraphs are very hard to understand just due to the language. The authors may want to consult a native speaker to polish the English further  Some of the minor issues: - The position of title and authors should be changed. - Some acronyms are used without any definitions, such as DRE, IDE, etc. - In section 2, “Distributed simulation” is listed twice. - In section 4.2, (2) of “There are a lot of off-the-shelf RTI implementations (2) ~” means Table 2? - In section 4.4, “CERTI RTI” should be modified to “CERTI”  **You may upload a PDF file with further comments for the authors.**   |  |  | | --- | --- | | **Review of con310s2 by Reviewer 2** | [top](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "top) |   **Summary**  The paper describes an architecture for the generation, verification, and distributed simulation of hardware-in-the-loop simulatioj models based on the HLA. The describes approach uses a mix of readily available components, components that had to be adapted and components especially developed for the proposed purpose. The paper inlucdes a case study that primarily appears to focus on verification abilities.  **Originality**  Using HLA in the context of hardware-in-the-loop and real time systems is not very popular and - in practice - possible only since a relatively short period of time. Consequently, work in this direction, showing the actual feasability delivers novel contributions to the field.  **Impact**  Hard to judge, because only little technical detail is shown in the article (what were the problems and how could they be solved). So, personally, I find it hard to see what to actually learn from the paper.  **Please explain in detail your evaluation of the paper.**  The proposed architecture appears to be woth being published. However, I have some difficulties with this paper:  - Language has to be polished in order to increase readability (please let the paper go through the hands/eyes of a natove speaker)  - The actual research contribution should be pointes out more clearly. The paper has "HLA-BAsed Distributed [...] simulation..." in it, bus I do not really see much explanation of the way, HLA was integrated (or how HLA was used to integrate the components).  - Given the title and abstract of the paper, there is too much focus on the verifiation abilities of the architecture (Section 6 as well as the focus of the case study).  Only if these changes could be made, I'd find the paper useful/readable.  **You may upload a PDF file with further comments for the authors.**   |  |  | | --- | --- | | **Review of con310s2 by Reviewer 3** | [top](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "top) |   **Summary**  this paper presents an environment for writing and testing real-time embedded systems.  **Originality**  The framework integrates verification methods with UML and other formatted languages.  **Impact**  The impact on the field is potentially high but as written it is low. The authors do not highlight contributions and the work is dating from 2002  **Please explain in detail your evaluation of the paper.**  The paper presents a framework generated from several old and new projcts. The framework is very useful but they failed to show the contribution of their work to the body of knowledge and the application example is at a small scale. I appears that there is more to this paper than presented here. As a result, I recommend it as a poster.  **You may upload a PDF file with further comments for the authors.**   |  |  | | --- | --- | | **Committee Comments to Authors:** | [top](https://ssl.linklings.net/conferences/wsc/?args=zYprcnt3D40tprcnt3DArQbCzprcnt3DHzGMTrJUHtGAX0zU3z0IQ3TzU30CxGtprcnt3DHhNMz9THQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTrAprcnt3DxGAX0zU3z0IQ3TtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGPCf40zU3b0bfPz" \l "top) |   None  Конец формы   |  |  |  | | --- | --- | --- | |  | Powered by [Linklings](http://www.linklings.com/" \t "_blank) | [Contact Support](https://ssl.linklings.net/conferences/wsc/?args=rJUHtGPCf40zU3b0bfPzTrAprcnt3DxGPCf40zU3b0bfPzTHQP0Aprcnt3DxfGzU3ACIIfb0HQP0Aprcnt3DxfTz0Cx0zfsGhaRTtUbprcnt3DsfGbprcnt3DsfNM_TzYprcnt3D40QHHGdbUfTtUbb0XfQbG4zt9MNhTzYprcnt3D40bprcnt3DQxGdbUfTzYprcnt3D40Iprcnt3Dxprcnt3DGdbUfTAprcnt3DxGzUyyfzICprcnt3DHz) | |